

U.S.P.T.O.
S/N 10/756,901

PATENT

JAN 19 2007

Applicant:
Serial No.:
Filed:
Title:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Paul A. Farrar Examiner: Sheila V. Clark
10/756,901 Group Art Unit: 2823
January 14, 2004 Docket: 303.572US2
SELECTIVE DEPOSITION OF SOLDER BALL CONTACTS

INFORMATION DISCLOSURE STATEMENT

MS RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. The Commissioner is hereby authorized to charge any required fees to Deposit Account No. 19-0743.

Pursuant to 37 C.F.R. 1.98(a)(2), Applicant believes that copies of cited U.S. Patents and Published Applications, and Non-Published Applications identifiable by USPTO Serial Number, are no longer required to be provided to the Office. Notification of this change to this effect was provided in the United States Patent and Trademark Office OG Notices dated October 12, 2004 and October 19, 2004. Thus, Applicant has not included copies of any US Patents or US Patent Applications identifiable by serial number that may be cited with this submission. Should the Office require copies to be provided, Applicant respectfully requests that notice of such requirement be directed to Applicant's below-signed representative. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

PAUL A. FARRAR

By his Representatives,

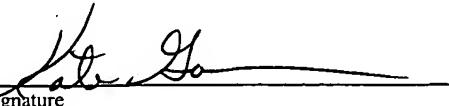
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6969

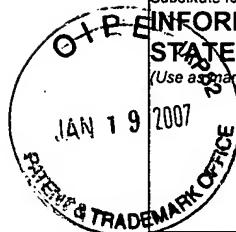
Date 1-16-07

By 
Viet V. Tong
Reg. No. 45,416

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 16 day of January 2007.

Name Kate Gannon


Signature



Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known Application Number 10/756,901 Filing Date January 14, 2004 First Named Inventor Farrar, Paul Group Art Unit 2823 Examiner Name Clark, Sheila		
Sheet 1 of 1		Attorney Docket No: 303.572US2		

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T ²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		BOHR, M. , "Interconnect scaling-the real limiter to high performance ULSI", <u>International Electron Devices Meeting, IEEE, (1995)</u> ,pp. 241-244	
		DAVIS, J. , et al., "A Priori Writing Estimation and Optimal Multilevel Wiring Networks for Portable ULSI Systems", <u>Electronic Components and Technology Conference, (1996)</u> ,pp. 1002-1008	
		GWENNAP, L. , "IC Makers Confront RC Limitations", <u>Microdesign Resources, Microprocessor Report,(1997)</u> ,pp. 14-18	
		KANTA, C. , et al., "Dual Damascene: A ULSI Wiring Technology", <u>VMIC Conference, (1991)</u> ,pp. 144-152	
		LAKSHMINARAYANAN, S. , <u>Multilevel Dual Damascene Copper Interconnections</u> , Rensselaer Polytechnic Institute, Ph.D Thesis,(1997),1-205	
		LICATA, T. , et al., "Dual Damascene Al Wiring for 256M DRAM", <u>Proceedings of the 12th International VLSI Multilevel Interconnection Conference, (1995)</u> ,pp. 596-602	
		LUTHER, B. , et al., "Planar Copper-Polyimide Back End of the Line Interconnections for ULSI Devices", <u>VMIC Conference, (1993)</u> ,pp. 15-21	
		RYAN, J. , et al., "The evolution of interconnection technology at IBM", <u>IBM J. Res. Develop., 39(4), (1995)</u> ,pp. 371-381	
		SINGER, P. , "New Interconnect Materials: Chasing the Promise of Faster Chips", <u>Semiconductor International, (1994)</u> ,pp. 52-56	
		TAUR, Y. , "CMOS scaling into the 21st century: 0.1 micrometer and beyond", <u>IBM J. Res. Develop., 39(1/2), (1995)</u> ,pp. 245-260	
		VOLLMER, B. , et al., "Recent advances in the application of collimated sputtering", <u>Thin Solid Films, 247, (1994)</u> ,pp. 104-111	

EXAMINER**DATE CONSIDERED**